



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Thomas P. Glenn, Steven Webster, Markus K. Liebhard
Assignee: Amkor Technology, Inc.
Title: CHIP SIZE IMAGE SENSOR WIREBOND PACKAGE FABRICATION METHOD
Serial No.: 09/712,314 Filed: November 13, 2000
Examiner: Alonzo Chambliss Group Art Unit: 2827
Docket No.: G0026M

Monterey, CA
January 8, 2003

CLEAN COPY OF DESCRIPTION REPLACEMENT PARAGRAPH(S)

IN THE ABSTRACT

Replace the paragraph extending from Page 38, line 7 to line 24 with:

--To form an image sensor package, a window is mounted above an active area on an upper surface of an image sensor. A noncritical region of the upper surface of the image sensor is between the active area and bond pads of the image sensor. A lower surface of a step up ring is mounted above the noncritical region of the upper surface of the image sensor. An upper surface of the step up ring includes a plurality of electrically conductive traces. Bond wires are formed between the bond pads of the image sensor and the electrically conductive traces on the upper surface of the step up ring. The step up ring is mounted so that the window is located in or adjacent a central aperture of the step up ring.--

IN THE DESCRIPTION

Replace the paragraph extending from Page 31, line 34 to Page 32, line 10 with:

--This application is related to Glenn et al., co-filed and commonly assigned U.S. Patent Application Serial No. 09/711,993, entitled "CHIP SIZE IMAGE SENSOR WIREBOND PACKAGE"; Glenn et al., co-filed and commonly assigned U.S. Patent Application Serial No. 09/712,313, entitled "CHIP SIZE IMAGE SENSOR BUMPED PACKAGE"; and Glenn et al., co-filed and commonly assigned U.S. Patent Application Serial No. 09/711,994, entitled "CHIP SIZE IMAGE SENSOR BUMPED PACKAGE FABRICATION METHOD", which are all herein incorporated by reference in their entireties.--

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on January 8, 2003.



Attorney for Applicant(s)

January 8, 2003

Date of Signature